REMARKS

This Amendment is in response to an Office action dated 7/2/2003. A response is due 10/2/2003, and can be extended. A request for extension of time, and fee, is included herewith.

Claims 23-58 are pending in the application.

Claims 37, 46 and **53** are ALLOWED.

Grounds of Rejection

¶3 Claims 23, 24, 26-28, 47 are rejected under 35 USC 103 (a) as being unpatentable over Gilson, in view of Hansen (USP 5,742,840).

¶4 Claims 24-28 are rejected under 35 USC 103 (a) as being unpatentable over Gilson and Hansen in view of Chang (USP 5,687,325)

¶5 Claims 29, 31, 33-36, 38, 40, 42-45, 50, 52, 56, 58 are rejected under 35 USC 103 (a) as being unpatentable over Gilson, in view of Halahmi (USP 5,887,179).

¶10 Claims 30, 39, 49 and 55 are rejected under 35 USC 103 (a) as being unpatentable over Gilson in view of Chang (USP 5,687,325) and Halahmi (USP 5,887,179).

¶11 Claims 32, 41, 51 and 57 are rejected under 35 USC 103 (a) as being unpatentable over Gilson.

¶12. Claims 48 ad 54 are rejected under 35 USC 102(e) as being anticipated by Gilson.

Traversing the Rejections

Claim 23, 24-28, 47, and 59 (new)

Claim 23 recites a block of reconfigurable logic incorporated on the IC chip; and a block of media processor with a virtual instruction set capable of implementing a variety of multimedia algorithms incorporated on the IC chip separately from the reconfigurable logic block.

As the Office Action admits, Gilson fails to disclose a block of media processor with a virtual instruction set capable of implementing a variety of multimedia algorithms incorporated on the IC chip. However, the Office Action asserts that Hansen discloses a media processor with a virtual instruction set capable of implementing a variety of multimedia algorithms.

For the following reason, applicant states that it would not have been obvious to combine the teachings of Gilson and Hansen.

Gilson states, "According to the present invention, an integrated circuit computing device is provided. This computing device is implemented in an FPGA such as the RAM-based XC3020 FPGA by XILINX. The number of logic blocks and routing resources available in the XILINX FPGA makes it well suited for implementing a simple microprocessor such as a RISC Processor. The RISC Processor is coupled to a unique instruction execution unit that can be configured to implement a variety of very complex operations in hardware. This is accomplished by dynamically reprogramming the FPGA such that the instruction execution unit is reconfigured to perform the appropriate operation while most of the remaining functions within the FPGA remain unaltered." (col. 4, lines 22-34)

Thus, in the integrated circuit computing device of Gilson, a simple microprocessor such as a RISC Processor is used in combination of a reconfigurable instruction execution unit that can be configured to implement a variety of very complex operations in hardware. In one specific implantation shown in Fig. 3, the functions of a very complex and sophisticated digital audio system can be implemented very simply and inexpensively using the computing device 10. (col. 8, lines 62-67)

In other words, the integrated circuit computing device of Gilson, which contains a simple microprocessor in combination of a reconfigurable instruction execution unit, is already capable to simply and inexpensively implement a variety of multimedia algorithms by reconfiguring the reconfigurable instruction execution unit.

On the other hand, the media processor 12 of Hansen handles a data stream of audio, video, graphics and network information all with the same processor. (col. 11, lines 19-21) The integrated media processor 12 may comprises an execution unit 100, which includes three main elements, i.e., a multiple precision arithmetic/logic unit ("ALU") 102, a programmable switch 104, and an extended math element 106. (col. 11, line 51 - col. 12, line 55)

Because the computing device 10 of Gilson already capable to implement a variety of multimedia algorithms, it is not necessary to combine some of the elements in the media processor 12 of Hansen. If such combination were made, the combined elements would be redundant with the Reconfigurable Instruction Execution Unit 16.

Such redundant combination would be unfavorable because of increased complexity and cost (larger chip) required to implement the redundant elements. Such redundant combination would significantly diminishes the advantage of Gilson, i.e., capable to simply and inexpensively implement functions of a very complex and sophisticated system by using a simple microprocessor in combination of a reconfigurable instruction execution unit.

A skilled person would not have been motivated to make such redundant and unfavorable combination.

The inventors of this application conceived that, even if a block of media processor with a virtual instruction set capable of implementing a variety of multimedia algorithms is incorporated on an IC chip, it is advantageous to further incorporate a block of reconfigurable logic on the IC chip. The reconfigurable logic block may contain a "least common denominator" set of instructions for operating the media processor and managing communications between other reconfigurable portions of the logic block. See page 14, lines 6-9 of the specification.

Such combination of the block of media processor and the reconfigurable logic block is not disclosed in any of the cited references.

Claims 24-28, 47, and 59 depend on **claim 23**. These claims should also be allowable.

Claims 35 and 44

The programmable memory interface (PMI) core recited in these claims communicate with off-chip memory and configures it virtually into what is optimal for an application that demands non-standard size memory.

None of the cited references disclose this feature.

By means of this PMI core, for example, i) the external memory can be virtually configured so that one set of frame information can be sprit over one or more types (or chips) of memory, ii) for compressed data, the PMI can direct primary points to be stored in one off-chip memory while directing vectors to be stored in another off-chip memory, or iii) for mixed media, the audio portion can be stored in one off-chip memory and the video portion can be stored in another off-chip memory. See specification page 14, lines 14-24.

Claims 48 and 54

These claims recite an analog interface incorporated on the IC chip.

None of the cited references disclose this feature.

Gilson discloses, in Fig. 3, an expansion card 60 that contains a computing device 10, which is comprised of a Digital Signal Processor 70 implemented using the RISC Processor 14 and Reconfigurable Instruction Execution Unit 16 as shown in Fig. 1. The expansion card 60 also contains an audio input portion 69 and an Analog Output Portion 94. The audio input portion 69 includes a Dual 18-bit Analog-to-Digital (A/D) Converter 90, and the Analog Output Portion 94 includes an 18-bit Dual Digital to Analog (D/A) converter 96.

However, the computing device 10, which is an IC chip containing the RISC Processor 14 and Reconfigurable Instruction Execution Unit 16, does not have an analog interface.

That is, the A/D Converter 90 converts the analog input signal to a digital representation, which is then transferred to DSP 70. And the DSP 70 outputs a processed digital representation of the audio data to the D/A converter 96.

Thus, the computing device 10 only has a digital input and a digital output.

Claims 29-33, 38-42, 52, and 58, and claims 34, 36, 43, and 45

Claims 29-33, 38-42, 52, and 58 are amended to depend on allowable claim 37 or 46. By the amendment of these claims, claims 34, 36, 43 and 45 also become dependent on allowable claim 37 or 46.

These claims should also be allowable.

Newly-Presented Claims
Claim Count

The highest number of claims previously paid for is:
36 total claims (numbered 23-58)
19 independent claims

After entry of this Amendment, there will be
31 total claims (23-58, plus one, minus six cancelled)
19 independent claims (23,29,30,31,32, 33,35,37,38,39, 40,41,42,44,46, 48,62,54,58)

Thereby necessitating fees for
0 excess total @ $ 18 = 0
0 excess independent @ $86 = 0

Conclusion

The claims should be allowed.

A two month extension of time is necessitated, and is hereby requested.
A fee of $420 is enclosed herewith.

For the Applicant

Gerald E. Linden 11/15/03

Gerald E. Linden 30,282 date
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